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**BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES**

Application Number: 10/788,805
Filing Date: February 27, 2004
Appellant(s): LINDSTEDT, REIDAR

Ira S. Matsil
For Appellant

MAILED

APR 05 2007

EXAMINER'S ANSWER

GROUP 2800

This is in response to the appeal brief filed 12/19/06 appealing from the Office action mailed 02/24/06.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

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(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5,834,162	MALBA	11-1998
6,518,659	GLENN	2-2003

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4 and 25 are rejected under 35 U.S.C. 102(b) as being anticipated by Malba (PN 5,834,162).

Malba discloses, as shown in Figures 1-3, a semiconductor chip arrangement comprising:

- a mount element (substrate, not shown, Col. 4, lines 28-41 or bottom 10);
- a first semiconductor substrate (bottom 10 or middle 10) including at least one interconnect (14) formed on the first semiconductor substrate and also including at least one

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contact area (17) that is electrically connected to the interconnect and is arranged on a side surface of the first semiconductor substrate; and

a second semiconductor substrate (middle 10 or top 10) having at least one interconnect (14) formed on the second semiconductor substrate and also including at least one contact area (17) that is electrically connected to the interconnect and is arranged on a side surface of the second semiconductor substrate;

wherein the second semiconductor substrate is arranged on the first semiconductor substrate and the first semiconductor substrate is arranged on the mount element such that a first main surface of the second semiconductor substrate rests on the first semiconductor substrate, and a first main surface of the first semiconductor substrate rests on the mount element, and wherein an electrical contact is produced between the contact area on the first semiconductor substrate and the contact area on the second semiconductor substrate and wherein the first and second semiconductor substrates each comprise an unpackaged semiconductor chip with integrated circuitry disposed therein. Col. 4, lines 18-27 and Col. 5, lines 44-56.

Regarding claim 2, Malba discloses the first and second semiconductor substrates each have an integrated circuit disposed in the area of the first main surface, wherein, for both the first and second semiconductor substrates, the integrated circuit is electrically coupled to the interconnect.

Regarding claim 3, Malba discloses the semiconductor chip arrangement further comprising a conductive material (13) applied between the contact area on the first semiconductor substrate and the contact area on the second semiconductor substrate.

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Regarding claim 4, Malba discloses the first main surface of the first semiconductor substrate is attached to the mount element.

Regarding claim 25, Malba discloses the second semiconductor substrate is arranged in direct contact with the first semiconductor substrate and the first semiconductor substrate is arranged in direct contact with the mount element.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 5-7, 9-13, 20-25 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Malba (PN 5,834,162) in view of Glenn (PN 6,518,659).

Regarding claim 7, Malba discloses, as shown in Figures 1-3, a semiconductor chip arrangement comprising:

a second semiconductor substrate (bottom 10) including at least one interconnect (14) formed thereon, the second semiconductor substrate further including at least one contact area (17) that is electrically connected to the interconnect and is arranged along a side surface of the second semiconductor substrate; and

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a third semiconductor substrate (middle 10) arranged over the second semiconductor substrate, the third semiconductor substrate including at least one interconnect (14) formed thereon, the third semiconductor substrate further including at least one contact area (17) that is electrically connected to the interconnect and is arranged along a side surface of the third semiconductor substrate, the third semiconductor substrate arranged so that an electrical contact is produced between the contact area of the third semiconductor substrate and the contact area of the second semiconductor substrate.

Malba further discloses the chips can stack on each other to form the stack chip and that other chips (the first semiconductor substrate) can be formed adjacent the stack chips due to the sidewall bond pads (17). Col. 4, lines 18-27. Malba does not clearly show the second semiconductor substrate arranged so that an electrical contact is produced between the contact area of the first semiconductor substrate and the contact area of the second semiconductor substrate and the first, second and third semiconductor substrates forms on a mount element.

However, Glenn disclose a mount element (not shown, 31) having the first, second, and third semiconductor substrates (44,44,44) form thereon and the second semiconductor substrate arranged so that an electrical contact is produced between the contact area (23) of the first semiconductor substrate and the contact area (23) of the second semiconductor substrate. Note Figures 1 and 6A-6D of Glenn. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the structure of Malba having the first, second, and third semiconductor substrates form on the mount element, and the second semiconductor substrate arranged so that an electrical contact is produced between the contact area of the first semiconductor substrate and the contact area of the second semiconductor substrate, such as

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taught by Glenn in order to easily add more semiconductor substrate/chip to increase the circuit density without increasing the mounting area on a printed circuit board.

Regarding claim 9, Malba and Glen disclose the semiconductor chip arrangement further comprising a conductive material (at side 14) applied between the contact area (23) on the first semiconductor substrate and the contact area (23) on the second semiconductor substrate. Col. 5, lines 50-53 of Glenn, a conductive material (solder).

Regarding claim 10, Malba and Glen disclose the first semiconductor substrate is attached to the mount element and wherein the second semiconductor substrate is attached to the mount element (31). Figures 1 and 6A-6D of Glenn.

Regarding claims 5, 11 and 24, Malba and Glen disclose the contact areas on the first and the second semiconductor substrates each extend from a first main surface to a second main surface of the respective semiconductor substrate. Figures 1 and 6A-6D of Glenn.

Regarding claim 12, Malba and Glen disclose the contact area (23) on the third semiconductor substrate extends to a first main surface on the third semiconductor substrate.

Regarding claims 6, 13 and 25, Malba and Glen disclose each of the first, second, and third semiconductor substrates includes a dynamic random access memory formed therein.

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Regarding claim 21, Malba and Glen disclose each of the integrated circuitry is electrically coupled to the interconnect.

Regarding claim 22, Malba and Glen disclose the semiconductor chip arrangement further comprising a conductive material (at side 14) applied between the contact area on the first semiconductor substrate and the contact area on the second semiconductor substrate. Col. 5, lines 50-53 of Glenn, a conductive material (solder).

Regarding claim 23, Malba and Glen disclose the first semiconductor substrate is attached to the mount element and wherein the second semiconductor substrate is attached to the mount element. Figures 1 and 6A-6D of Glenn.

Regarding claim 27, Malba and Glen disclose the first semiconductor substrate is arranged in direct contact with the surface of the mount element, the second semiconductor substrate arranged in direct contact with the surface of the mount element, and the third semiconductor substrate is arranged in direct contact with the second semiconductor substrate. Figures 1 and 6A-6D of Glenn.

(10) Response to Argument

1. Appellant argues that Malba states electrical interconnect between the sidewall bond pads 17 of the various chips can be made, but does not state where the electrical interconnects are

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between because claim 1 requires an electrical contact between the contact area on the first semiconductor substrate and the contact area on the second semiconductor substrate. This argument is not convincing for the following reasons: first, Appellant admits that Malba states electrical interconnect between the sidewall bond pads 17 of the various chips can be made. Second, Malba discloses, at Col. 4, lines 18-27, Col. 5, lines 52-56 and Claim 13, that stacking the chips one on top of another so the chips can be interconnected.

2. Appellant argues that Malba does not disclose a conductive material applied between the contact area on the first semiconductor substrate and the contact area on the second semiconductor substrate. This argument is not convincing because Malba clearly disclose the conductive material (13) applied between the contact area on the first semiconductor substrate and the contact area on the second semiconductor substrate. Note that the claimed does not specifically states it is directly between the contact areas.

3. Appellant argues that Malba discloses the chips are stacked but does not disclose the first main surface of the middle chip 10 is attached to the lowest chip 10, which is not the same like the present invention which teaches that the first semiconductor substrate may be fixed on the mount element by means of an adhesive or via electrical contact for example by means of soldered joints or mechanical joints. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., may be fixed on the mount element by means of an adhesive or via electrical contact for example by means of soldered joints or mechanical joints) are not recited in

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the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). According to Merriam Webster's Collegiate Dictionary, the word "attached" is defined as to bring (oneself) into an association. As in this case, stacking of the chips mean to bring one chip on top of (or into an association with) another chip. This also means to bring the first main surface of the middle chip on top of (or into an association with) the lowest chip.

4. Appellant argues that the references do not teach the contact area on the first semiconductor substrate and contact area on the second semiconductor substrate each extend from the first main surface to a second main surface of the respective semiconductor substrate. This argument is not convincing because Malba discloses, at Col. 5, lines 44-56, that the process (of L-connects) can be utilized using any desired interconnect configuration or combination of interconnect configurations whereby bond pads on a top surface of a chip are extended to an edge or sidewall of the chip, which enables stacking of the chips, interconnection of the chip to other components, and/or packaging of stacked chips to other stacked chips or components. Glenn, on the other hand, discloses, as shown in Figures 6A-6D, the interconnection of stacked chips to other stacked chips having the contact area (23) extending from a first main surface to a second main surface. Therefore, the combination is proper.

Appellant argues that the contents of the two cited references do not provide any suggestion for combining their technical teaching since Glenn refers to a packaged semiconductor substrate surrounded by a housing and Malba refers to an unpackaged

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semiconductor substrate, because it is not apparent how one of ordinary skill in the art would apply the electrical contacts 21 of Glenn to the unpackage chip of Malba. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Malba discloses, at Col. 4, lines 18-27, that with the chips stacked, packaging of the stacked chips with other chips can be readily accomplished due to the sidewall bond pads (17). This means the chips stack one on top of another to form the stacked chips and other chips can be formed adjacent to the stacked chips due to the sidewall bond pads (17). However, Malba does not show or express this disclosure into the drawings. That is the reason why Glenn is brought up to show in drawings (Figures 6C-6D) how the stacked chips and other chips can be formed adjacent to each other due to the sidewall contact area (23).

5. Appellant argues that the references are not properly combinable for the reason as state in number 4, and the combination of Malba and Glenn does not teach two substrates alongside each other on the mount element. This argument is not convincing for the following reasons: first, as explained above, the references are properly combinable. Second, Glenn discloses, as shown in Figure 6A, the chip stack 50 forms on the mount element 31. Glen further discloses, at Col. 2, lines 17-20, that one chip stack may be placed next to another on a mount element. Figure 6D

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shows two chip stack 50 alongside or next to each other. Therefore, it is inherent that Figure 6D of Glen shows two substrates (44) alongside each other on the mount element.

6. Appellant argues that the references do not teach a conductive material applied between the contact area on the first semiconductor substrate and the contact area on the second semiconductor substrate because the L-connect 14 couples the top surface bond pad of a chip to the sidewall bond pad 17 of that same chip is in no way a conductive material applied between the contact area on the first semiconductor substrate and the contact area on the second semiconductor substrate. This argument is not convincing because Glenn discloses, as shown in Figures 1, 6D and Col. 5, lines 50-53, a conductive material (solder, at side 14) is between the contact area (23) on the first semiconductor substrate and the contact area (23) on the second semiconductor substrate.

7. Appellant argues that the references do not teach the contact area on the first semiconductor substrate and contact area on the second semiconductor substrate each extend from the first main surface to a second main surface of the respective semiconductor substrate. This argument is not convincing because for the reason as stated above, since Malba discloses, at Col. 5, lines 44-56, that the process (of L-connects) can be utilized using any desired interconnect configuration or combination of interconnect configurations whereby bond pads on a top surface of a chip are extended to an edge or sidewall of the chip, which enables stacking of the chips, interconnection of the chip to other components, and/or packaging of stacked chips to other stacked chips or components. Glenn, on the other hand, discloses, as shown in Figures 6A-

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6D, the interconnection of stacked chips to other stacked chips having the contact area (23) extending from a first main surface to a second main surface.

8. Appellant argues that the references are not properly combinable and the combination of Malba and Glenn does not teach the mount element for the reason as state in number 5. This argument is not convincing for the reasons as explained in numbers 4 and 5.

9. Appellant argues that the references do not teach a conductive material applied between the contact area on the first semiconductor substrate and the contact area on the second semiconductor substrate because the L-connect 14 couples the top surface bond pad of a chip to the sidewall bond pad 17 of that same chip is in no way a conductive material applied between the contact area on the first semiconductor substrate and the contact area on the second semiconductor substrate. This argument in not convincing because Glenn discloses, as shown in Figures 1, 6D and Col. 5, lines 50-53, a conductive material (solder, at side 14) is between the contact area (23) on the first semiconductor substrate and the contact area (23) on the second semiconductor substrate.

10. Appellant argues that the references do not teach the contact area on the first semiconductor substrate and contact area on the second semiconductor substrate each extend from the first main surface to a second main surface of the respective semiconductor substrate. This argument is not convincing because for the reason as stated above, since Malba discloses, at Col. 5, lines 44-56, that the process (of L-connects) can be utilized using any desired

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interconnect configuration or combination of interconnect configurations whereby bond pads on a top surface of a chip are extended to an edge or sidewall of the chip, which enables stacking of the chips, interconnection of the chip to other components, and/or packaging of stacked chips to other stacked chips or components. Glenn, on the other hand, discloses, as shown in Figures 6A-6D, the interconnection of stacked chips to other stacked chips having the contact area (23) extending from a first main surface to a second main surface.

11. Appellant argues that the references do not teach the first semiconductor substrate is arranged in direct contact with the surface of the mount element and the second semiconductor substrate is arranged in direct contact with the surface of the mount element. This argument is not convincing because, as explained in number 5, the combination of Malba and Glenn shows the first semiconductor substrate is arranged over the surface of the mount element and the second semiconductor substrate is arranged over the surface of the mount element. Therefore, it is inherent that the combination of Malba and Glenn discloses the first semiconductor substrate is arranged in direct contact with the surface of the mount element and the second semiconductor substrate is arranged in direct contact with the surface of the mount element.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

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For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Hung Vu

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